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| Tool Version : Vivado v.2018.3 (win64) Build 2405991 Thu Dec 6 23:38:27 MST 2018

| Date : Thu Oct 17 09:48:55 2024

| Host : Samuel running 64-bit major release (build 9200)

| Command : report\_methodology -file hello\_world\_arty\_a7\_methodology\_drc\_routed.rpt -pb hello\_world\_arty\_a7\_methodology\_drc\_routed.pb -rpx hello\_world\_arty\_a7\_methodology\_drc\_routed.rpx

| Design : hello\_world\_arty\_a7

| Device : xc7a100ticsg324-1L

| Speed File : -1L

| Design State : Fully Routed

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Report Methodology

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1. REPORT SUMMARY

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Netlist: netlist

Floorplan: design\_1

Design limits: <entire design considered>

Max violations: <unlimited>

Violations found: 2

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| Rule | Severity | Description | Violations |

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2. REPORT DETAILS

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SYNTH-6#1 Warning

Timing of a block RAM might be sub-optimal

The timing for the instance rvsteel\_mcu\_instance/rvsteel\_ram\_instance/ram\_reg\_0, implemented as a block RAM, might be sub-optimal as no output register was merged into the block

Related violations: <none>

SYNTH-6#2 Warning

Timing of a block RAM might be sub-optimal

The timing for the instance rvsteel\_mcu\_instance/rvsteel\_ram\_instance/ram\_reg\_1, implemented as a block RAM, might be sub-optimal as no output register was merged into the block

Related violations: <none>